Analog-to-digital conversion (ADC) MEC100x-Lectures 7_2

Energy, Power and Intelligent Control

School of Electronics, Electrical Engineering and Computer Science

Ashby Building

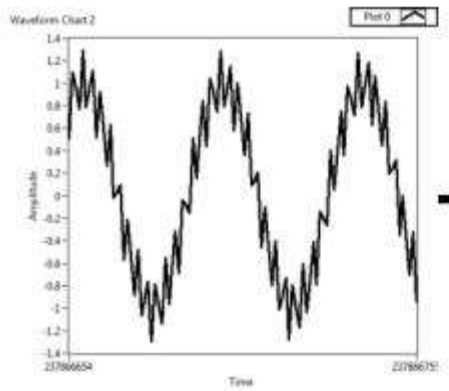
Queen's University Belfast

Aims

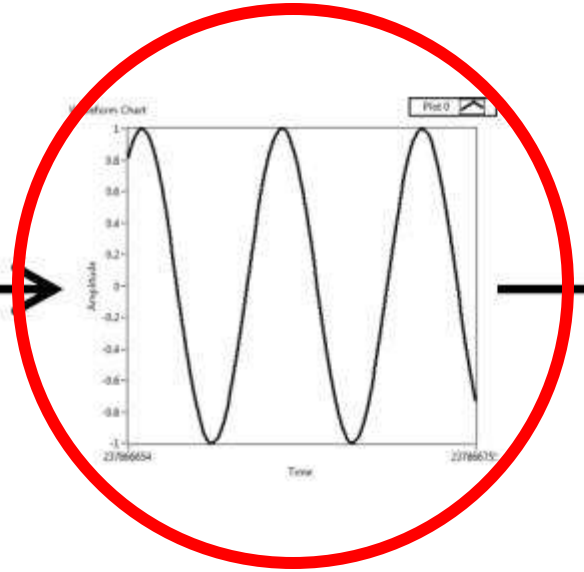
1. I/O Typical of ADC
2. Example of Shaft Encoder
3. I/O typical ADC (ADC0804-AD673)
4. Practice: Proteus implementation

ADC

Noisy

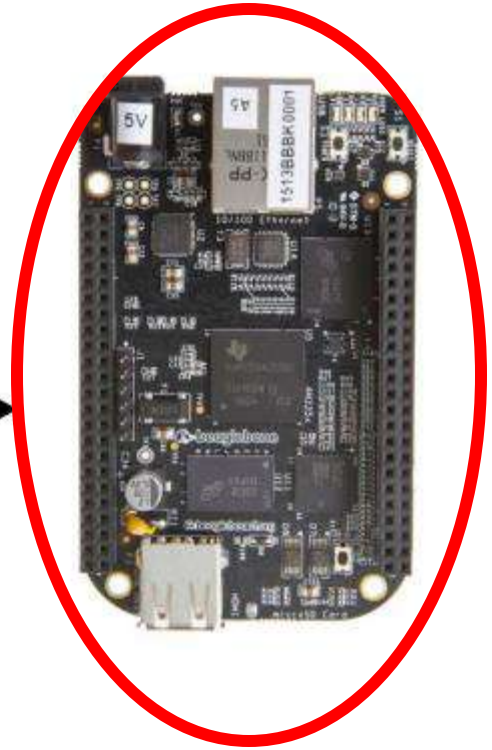


Analog to digital converter



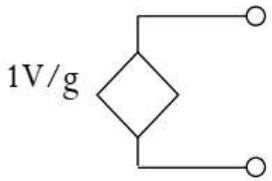
A/D

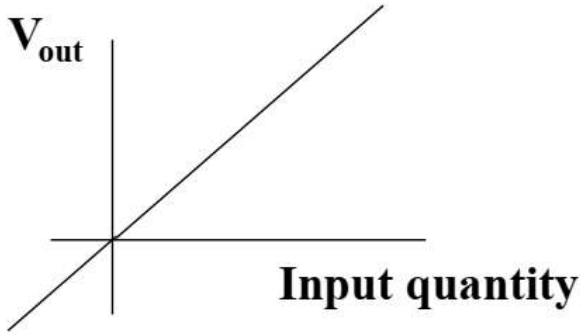
Beaglebone



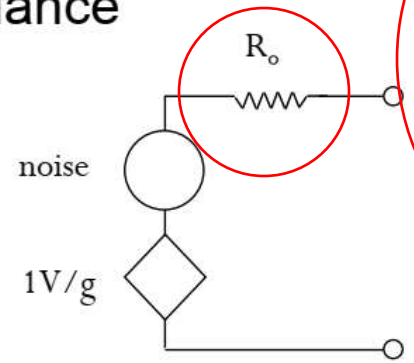
Signal Sources - 3

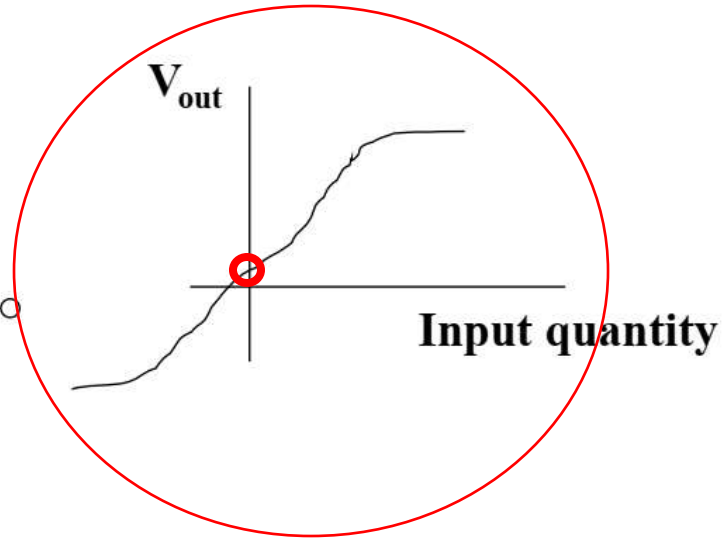
- Ideal signal source
  - Ideal voltage source
  - No output impedance





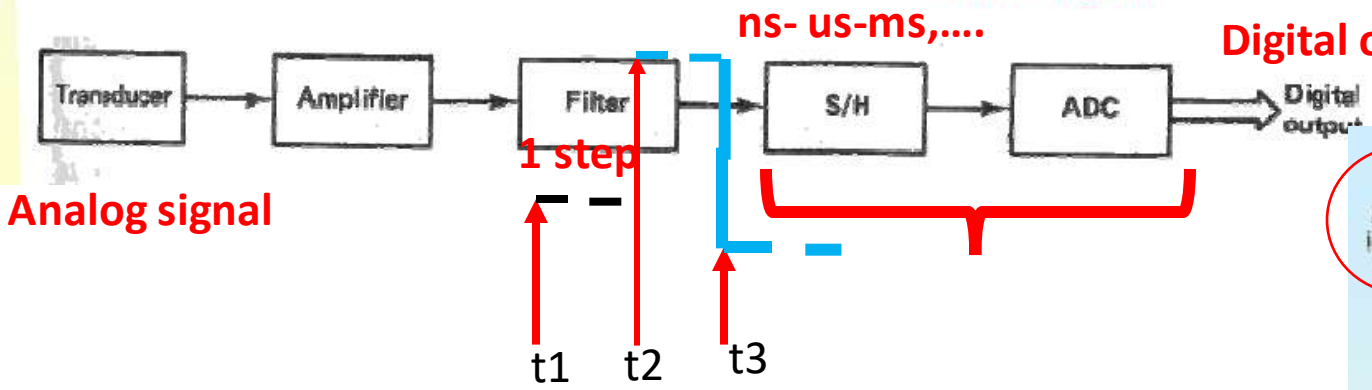
- Practical signal source
  - Relatively low-level output
  - Finite output impedance
  - Prone to noise
  - Zero offset
  - Non-linear



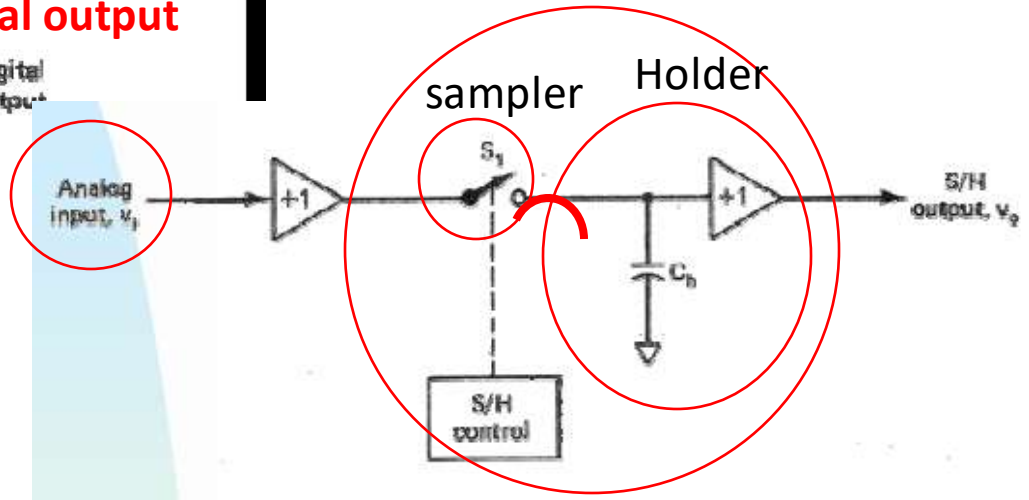


I. Single Channel System

- **Transducer**
  - Generate signal of low amplitude, mixed with undesirable noise
- **Amplifier, Filters**
  - Amplify
  - Remove noise
  - Linearize
- **S/H (Sample and Hold)**
  - Reduce uncertainty error in the converted output when input changes are fast compared to the conversion time
  - In Multi-channel system
    - To hold a sample from one channel while multiplexer proceed to sample next one
    - Simultaneous sampling of two signal



AD 582 ➡ ADC



Commercially available monolithic ADCs

Device type	Manufacturers	Resolution (bits)	Conversion method	Conversion time (μs)	Supply volts (V)	Features	Price (100s)
ADC0804	National, Intersil	8	Successive approx. (S.A.)	100	+5	CMOS on-chip clock and buffer	$ 3
AD7574	Analog Devices	8	S.A.	15	+5	Similar to ADC0804	7
AD570	Analog Devices	8	S.A.	25	+5, −15	On-chip clock reference, buffer, programmable input range	18
AD573/ AD673	Analog Devices	10/8	S.A.	15/20	+5, −15	On-chip clock reference, buffer, programmable input range	50
ADC1080/ 1280	National	10/12	S.A.	18/22	+5, ±15	Similar to AD570	—
TSC7109	Intersil, Teledyne	12 plus sign	Modified dual-slope	33 ms	+5	CMOS parallel/serial UART interface	15
AD7555	Analog Devices	4½ digits	Modified dual-slope	610 ms	±5	CMOS clock, buffer, parallel/serial	20
			Multiple inputs				
ADC0808	National, Texas Instruments	8	S.A.	100	+5	CMOS 8-channel AMUX, clock, buffer, address latch	8
AD7581	Analog Devices	8	S.A.	80	+5	CMOS 8-channel AMUX, clock, buffer, address latch	14
ADC0816	National, Texas Instruments	8	S.A.	100	+5	Like ADC0808 but 16-channel AMUX and easy S/H insert	14
			Flash ADCs				
AD9010/ AD9020	Analog Devices	6	Parallel	10 ns/ 20 ns	±5	For very high throughput	190/ 84
MC10317	Motorola	7	Parallel	30 ns	±5	ECL	—

Multi-Channel system

- **Analog multiplexer and a ADC**
  - Low cost

Why we use it?

When we are be going to have: A low cost ADC

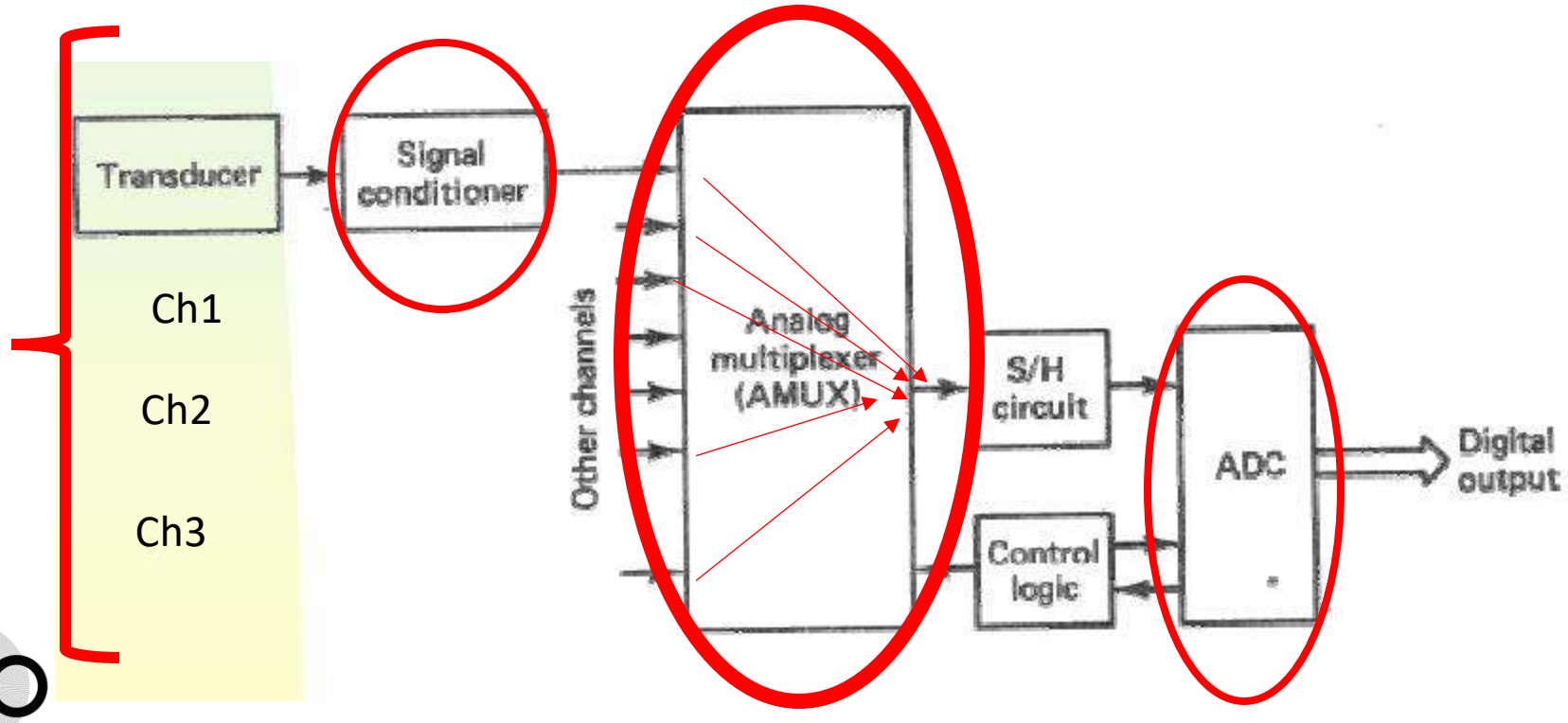
Where we can use it?

Cost-effective electronic circuit board

How we can use it?

Several analog output channel

Operation

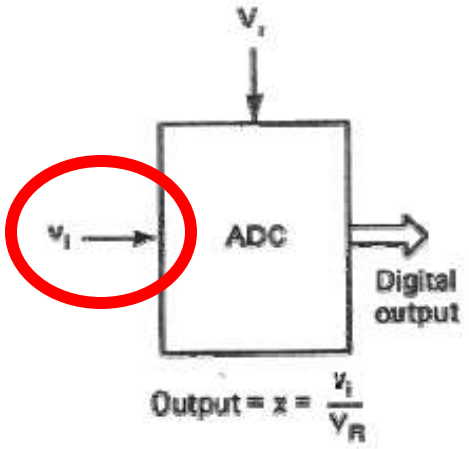


ANALOG

MICRO CONTROLLER

1. ADC Essentials

- **Basic I/O Relationship**
  - ADC is a Rationing System
    - x = Analog input / Reference
      - Fraction: 0 ~ 1

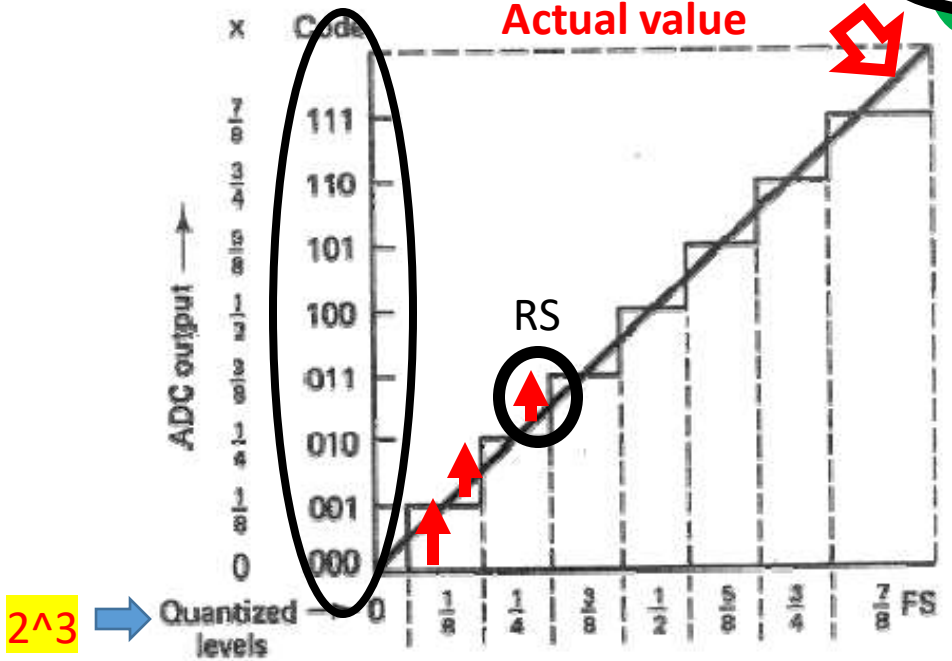


- **n bits ADC**
  - Number of discrete output level : 2^n
  - Quantization
    - LSB size
    - Q = LSB = FS / 2^n
- **Quantization Error**
  - ±1/2 LSB
  - Reduced by increasing n

Resolution: RS= Vfs/ 2^n

VFS=V Full scale:
10V /2^8= 0.03
5 V/2^8=0.01
1V/2^8=0.003
0.5V/2^8=0.0019

Actual value

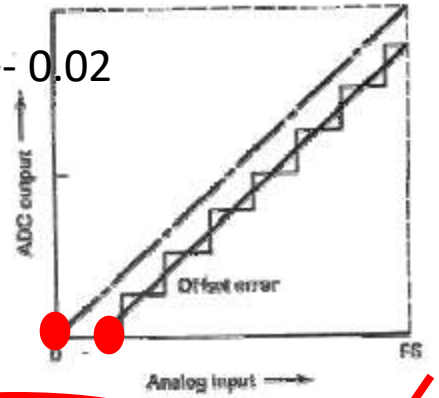


2^3

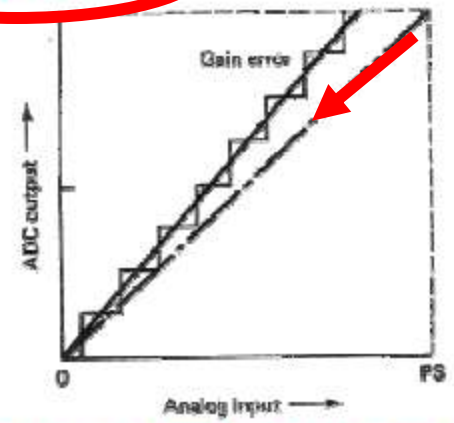
Converter Errors

- Offset Error

Programming: V+- 0.02

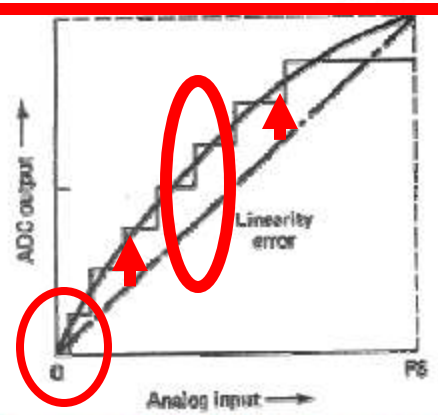


- Gain Error

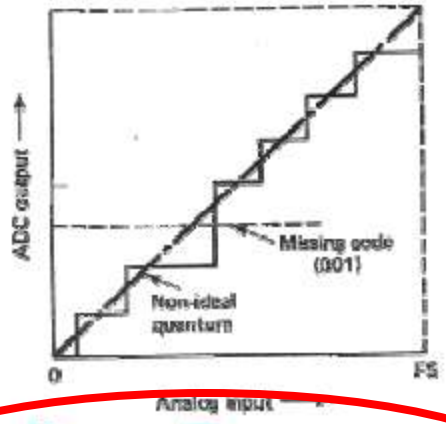


- Can be eliminated by initial adjustments

- Integral Linearity Error



- Differential Linearity Error



- Nonlinear Error
  - Hard to remove

What is ADC Resolution?

0000 0000 8 bit

Bits	Multiply	Decimal
2^1	2	2 (0-1)
2^2	2x2	4 (0-3)
2^3	2x2x2	8 (0-7)
2^4	2x2x2x2	16 (0-15)
2^5	2x2x2x2x2	32 (0-31)
2^6	2x2x2x2x2x2	64 (0-63)
2^7	2x2x2x2x2x2x2	128 (0-127)
2^8	2x2x2x2x2x2x2x2	256 (0-255)

2 Multiplied by itself at 8 times

Decimal equivalent

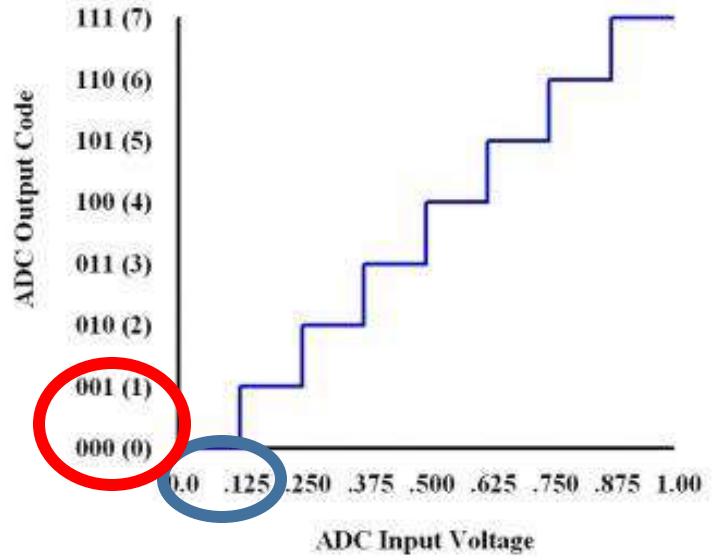
ADC resolution

The ADC resolution is defined as **the smallest incremental voltage that can be recognized and causes a change in the digital output**.

Smallest in ADC input voltage can cause a change in a digital output.

It is expressed as the number **of bits output by the ADC.**

Therefore, an ADC which **converts the analog signal to a 12-bit digital value, it has a resolution of 12 bits.**



Conversion Time

- Required time (tc) before the converter can provide valid output data

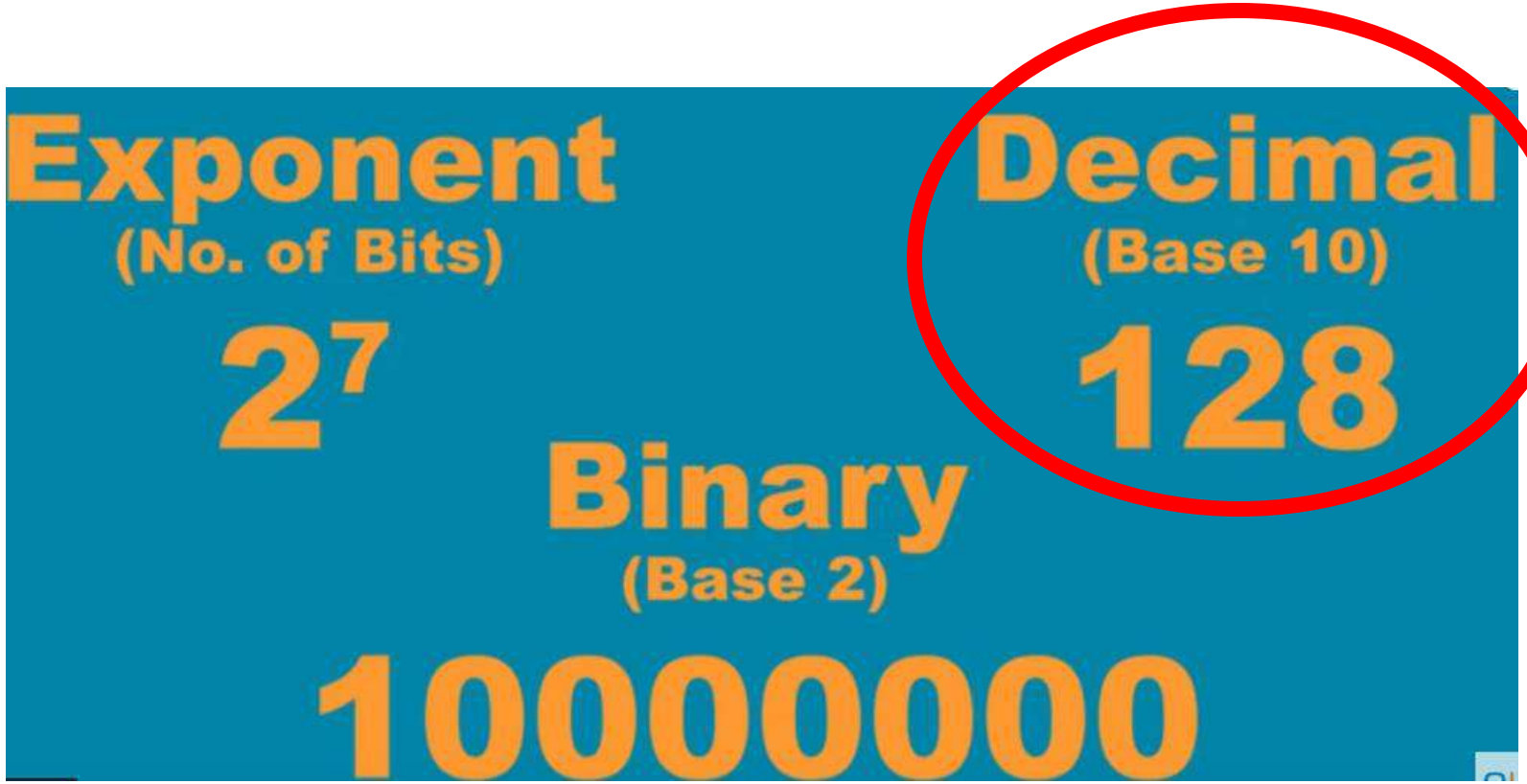
tc: Required time for conversion from ADC analog value to digital codes; It can be:

ms

µs

ns

ADC Resolution



Decimal equivalent

$$2^n$$

2 Multiplied by itself at 8 times

n: number of ADC bit

ADC Resolution

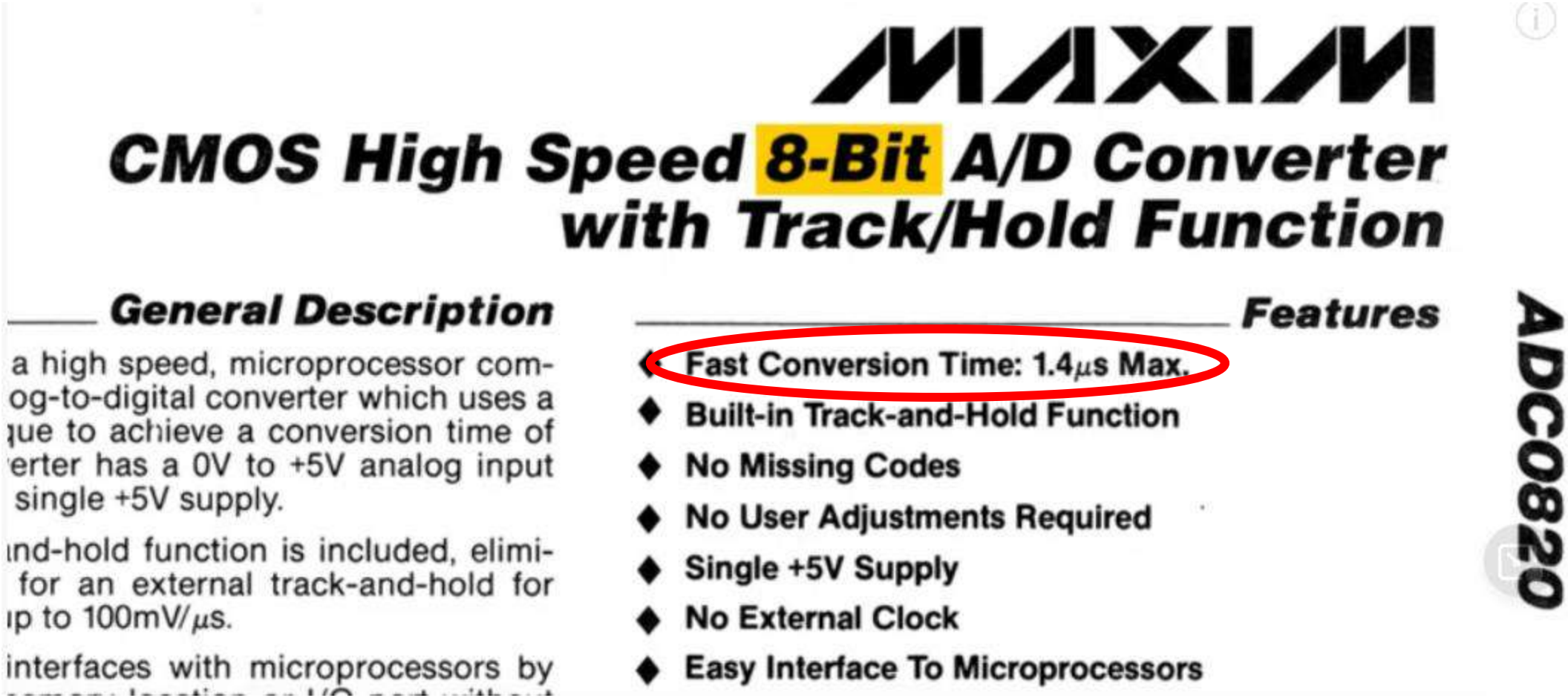
$$2^n$$

n: number of ADC bit

★ ADC Resolution

$$R.S = \frac{Vfs(full\ scale\ voltage)}{2^n}$$

❑ Analog to Digital converters start as low as 8 bit



MAXIM

CMOS High Speed 8-Bit A/D Converter with Track/Hold Function

ADC0820

General Description

a high speed, microprocessor com-
og-to-digital converter which uses a
ique to achieve a conversion time of
erter has a 0V to +5V analog input
single +5V supply.

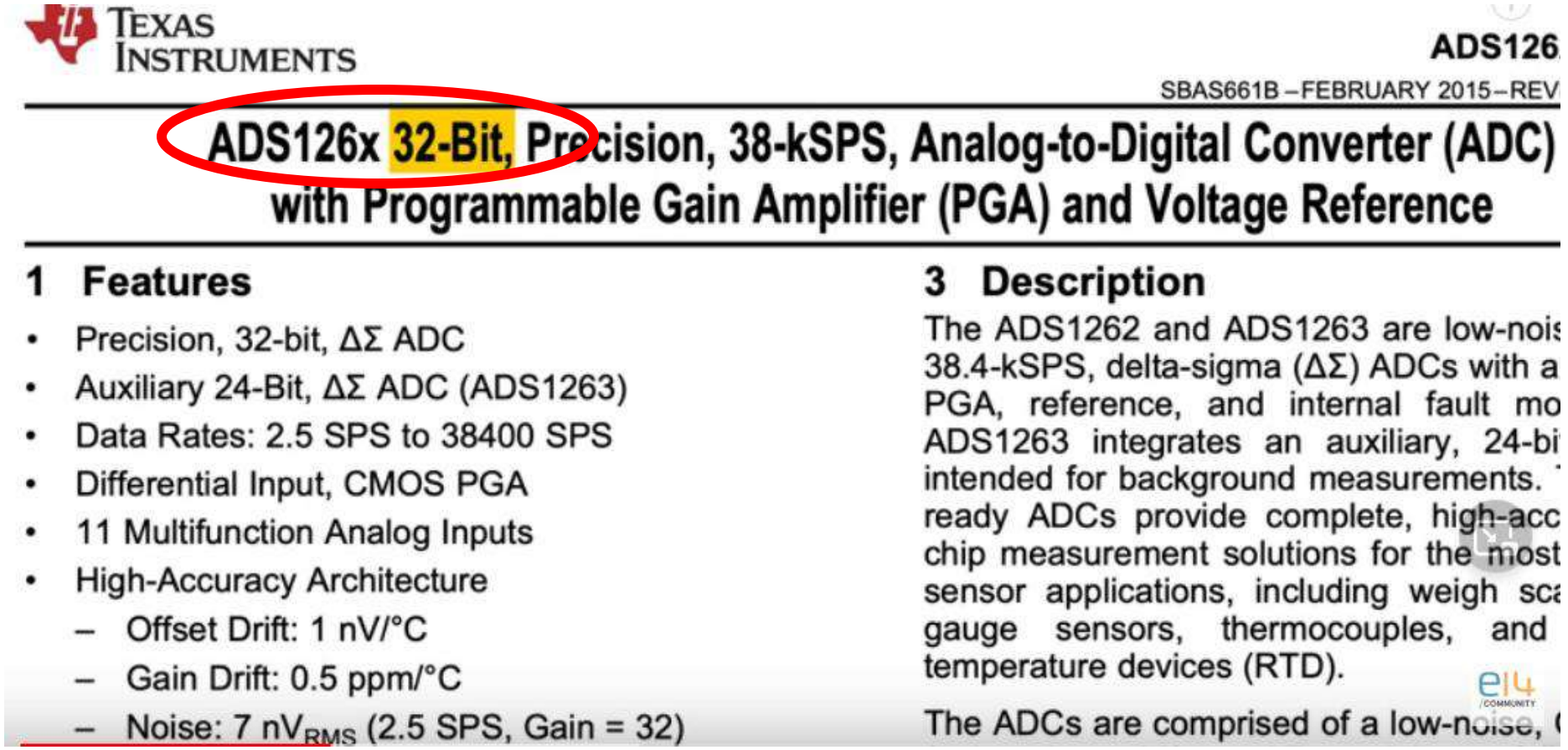
and-hold function is included, elimi-
for an external track-and-hold for
up to 100mV/μs.

interfaces with microprocessors by

Features

- Fast Conversion Time: 1.4μs Max.
- Built-in Track-and-Hold Function
- No Missing Codes
- No User Adjustments Required
- Single +5V Supply
- No External Clock
- Easy Interface To Microprocessors

❑ It can be found as high as 32 bit.



TEXAS INSTRUMENTS

ADS126

SBAS661B – FEBRUARY 2015 – REV

ADS126x 32-Bit, Precision, 38-kSPS, Analog-to-Digital Converter (ADC) with Programmable Gain Amplifier (PGA) and Voltage Reference

1 Features

- Precision, 32-bit, ΔΣ ADC
- Auxiliary 24-Bit, ΔΣ ADC (ADS1263)
- Data Rates: 2.5 SPS to 38400 SPS
- Differential Input, CMOS PGA
- 11 Multifunction Analog Inputs
- High-Accuracy Architecture
  - Offset Drift: 1 nV/°C
  - Gain Drift: 0.5 ppm/°C
  - Noise: 7 nV_{RMS} (2.5 SPS, Gain = 32)

3 Description

The ADS1262 and ADS1263 are low-nois
38.4-kSPS, delta-sigma (ΔΣ) ADCs with a
PGA, reference, and internal fault mo
ADS1263 integrates an auxiliary, 24-bi
intended for background measurements.
ready ADCs provide complete, high-acc
chip measurement solutions for the most
sensor applications, including weigh sca
gauge sensors, thermocouples, and
temperature devices (RTD).

The ADCs are comprised of a low-noise,

❑Most commonly 10; 12; 16 or 24 bits

MICROCHIP

MCP3002

2.7V Dual Channel 10-Bit A/D Converter with SPI Serial Interface

- 10-bit resolution
- ±1 LSB maximum DNL
- ±1 LSB maximum INL
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V

The MCP3002 is a successive approximation 10-bit analog-to-digital (A/D) converter with on-board sample and hold circuitry.

The MCP3002 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) are both specified at ±1 LSB. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device

maxim integrated

EVALUATION KIT AVAILABLE

MAX187/MAX189

+5V, Low-Power, 12-Bit Serial ADCs

General Description

The MAX187/MAX189 serial 12-bit analog-to-digital converters (ADCs) operate from a single +5V supply and accept a 0 to 5V analog input. Both parts feature an 8.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed 3-wire serial interface.

The MAX187/MAX189 digitize signals at a 75ksps throughput rate. An external clock accesses data from the interface, which communicates without external

Features

- ♦ 12-Bit Resolution
- ♦ ±½ LSB Integral Nonlinearity (MAX187A/MAX189A)
- ♦ Internal Track/Hold, 75kHz Sampling Rate
- ♦ Single +5V Operation
- ♦ Low Power: 2µA Shutdown Current
  1.5mA Operating Current
- ♦ Internal 4.096V Buffered Reference (MAX187)

ANALOG DEVICES

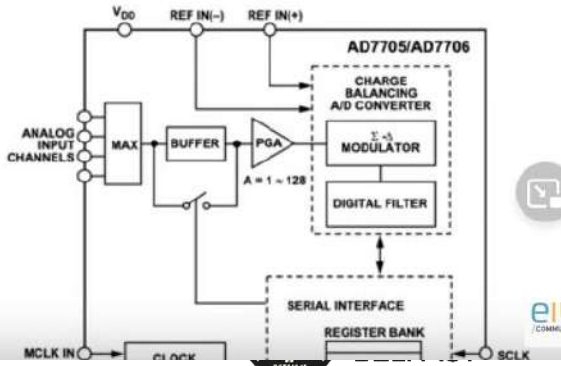
3 V/5 V, 1 mW, 2-/3-Channel, 16-Bit, Sigma-Delta ADCs

AD7705/AD7706

FEATURES

AD7705: 2 fully differential input channel ADCs
AD7706: 3 pseudo differential input channel ADCs
16 bits no missing codes
0.003% nonlinearity
Programmable gain front end: gains from 1 to 128
3-wire serial interface
SPI®-, QSPI™-, MICROWIRE™-, and DSP-compatible
Schmitt-trigger input on SCLK
Ability to buffer the analog input
2.7 V to 3.3 V or 4.75 V to 5.25 V operation
Power dissipation 1 mW maximum @ 3 V
Standby current 8 µA maximum
16-lead PDIP, 16-lead SOIC, and 16-lead TSSOP packages

FUNCTIONAL BLOCK DIAGRAM



- **S/H (Sample and Hold)**
  - Analog circuits that quickly samples the input signal on command and then holds it relatively constant while the ADC performs conversion

Analog Input Signal

ADC 0804
Vfs= 0-5V
n=8 bit
R.S=5/2^8=5/256=0.0195
RS= 1.25/256=???

- **Typically, Differential or Single-ended input signal of a single polarity**
  - Typical Input Range
    - 0 ~ 10V and 0 ~ 5V
  - If Actual input signal does not span Full Input range
    - Some of the converter output code never used
    - Waste of converter dynamic range
    - Greater relative effects of the converter errors

0-1.25
0-0.5
0-2.5
Vfs

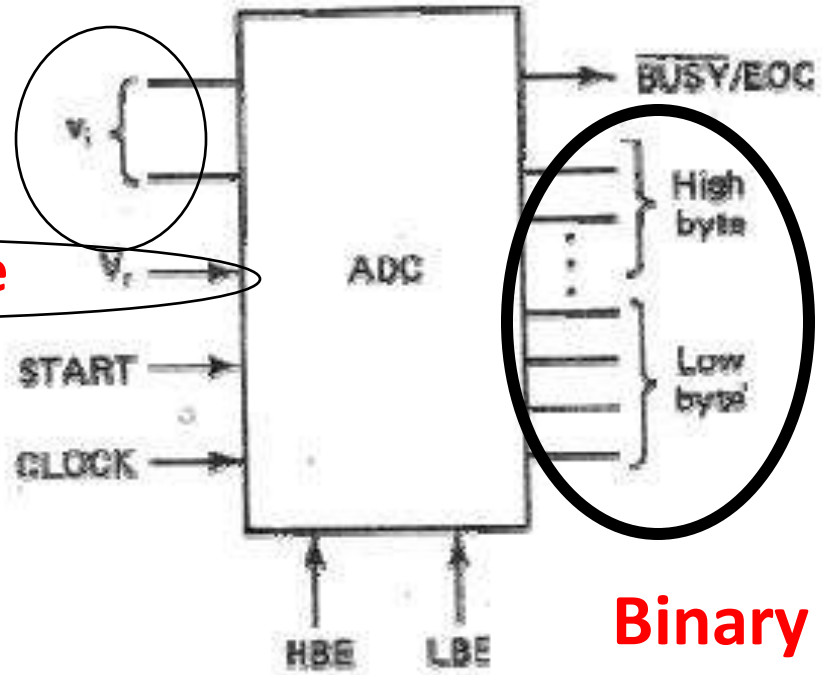
- **Matching input signal and input range**
  - Prescaling input signal using OP Amp
    - In a final stage of preconditioning circuit
  - By proportionally scaling down the reference signal
    - If reference signal is adjustable

RS=Vfs / (2^n=bit A/D)

I/O of typical ADC

Input voltage

Reference voltage



Binary

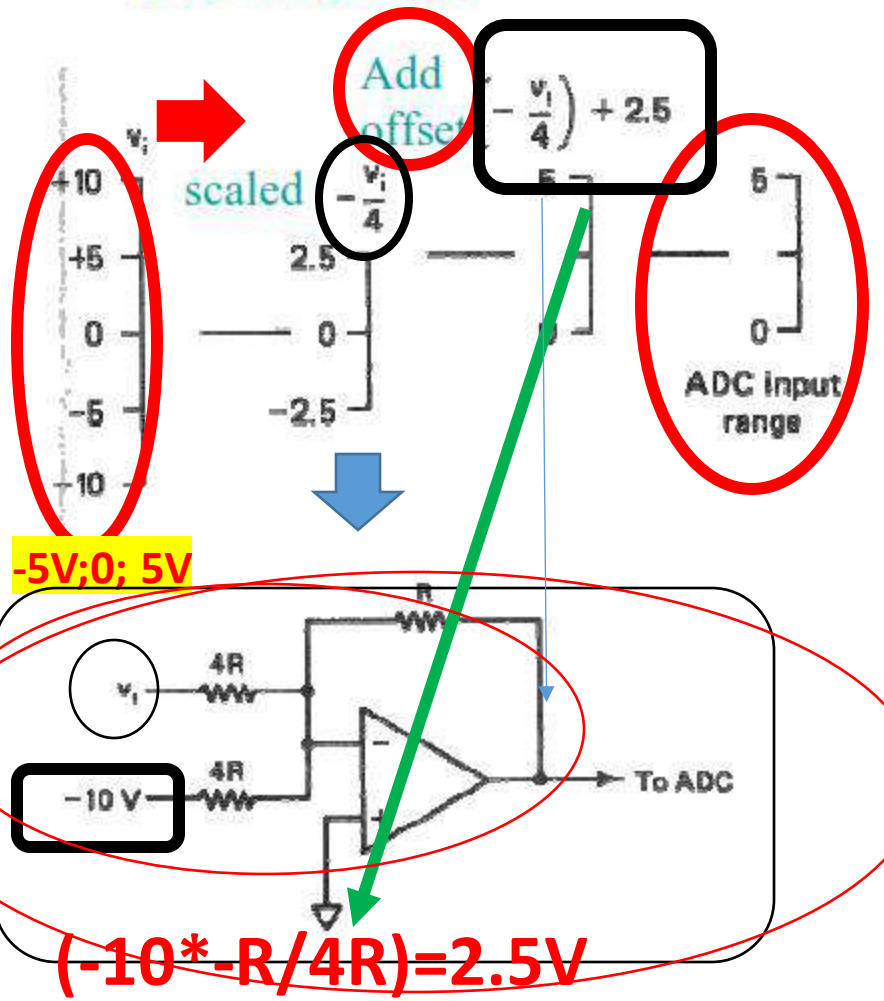
ADC output

- Number of bits
  - 8 and 12 bits are typica
  - 10, 14, 16 bits also available

Converting bipolar to unipolar

- Using unipolar converter when input signal is bipolar
  - Scaling down the input
  - Adding an offset
- Bipolar Converter
  - If polarity information in output is desired
  - Bipolar input range
    - Typically, 0 ~ ±5V
  - Bipolar Output
    - 2's Complement
    - Offset Binary
    - Sign Magnitude

- Input signal is scaled and an offset is added



A/D=== 0-5 VDC

0-5V DC===A/D

ADC 0805 Data Sheet

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

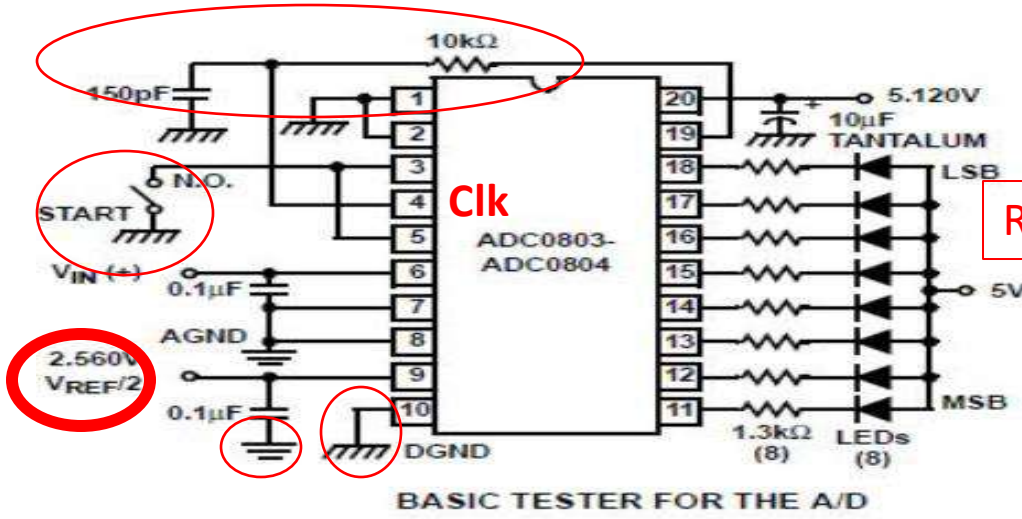
- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

Resolution	8 bits
Total error	±¼ LSB, ±½ LSB and ±1 LSB
Conversion time	100 μs

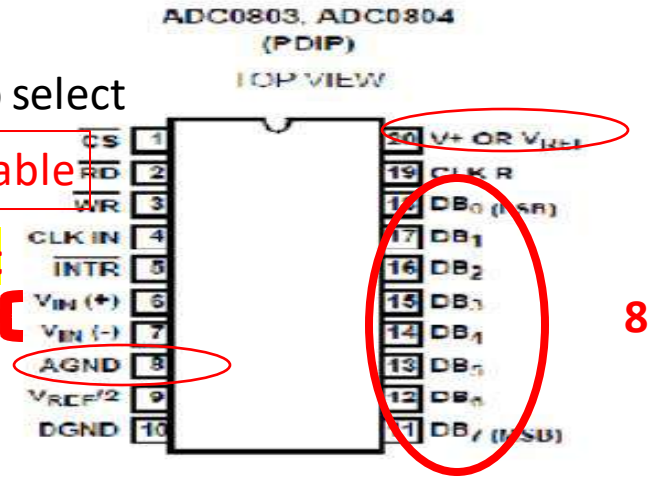
8 bit

مشخصات آی سی ADC0804:



BASIC TESTER FOR THE A/D

Pinout



Chip select

Read==enable

interrupt

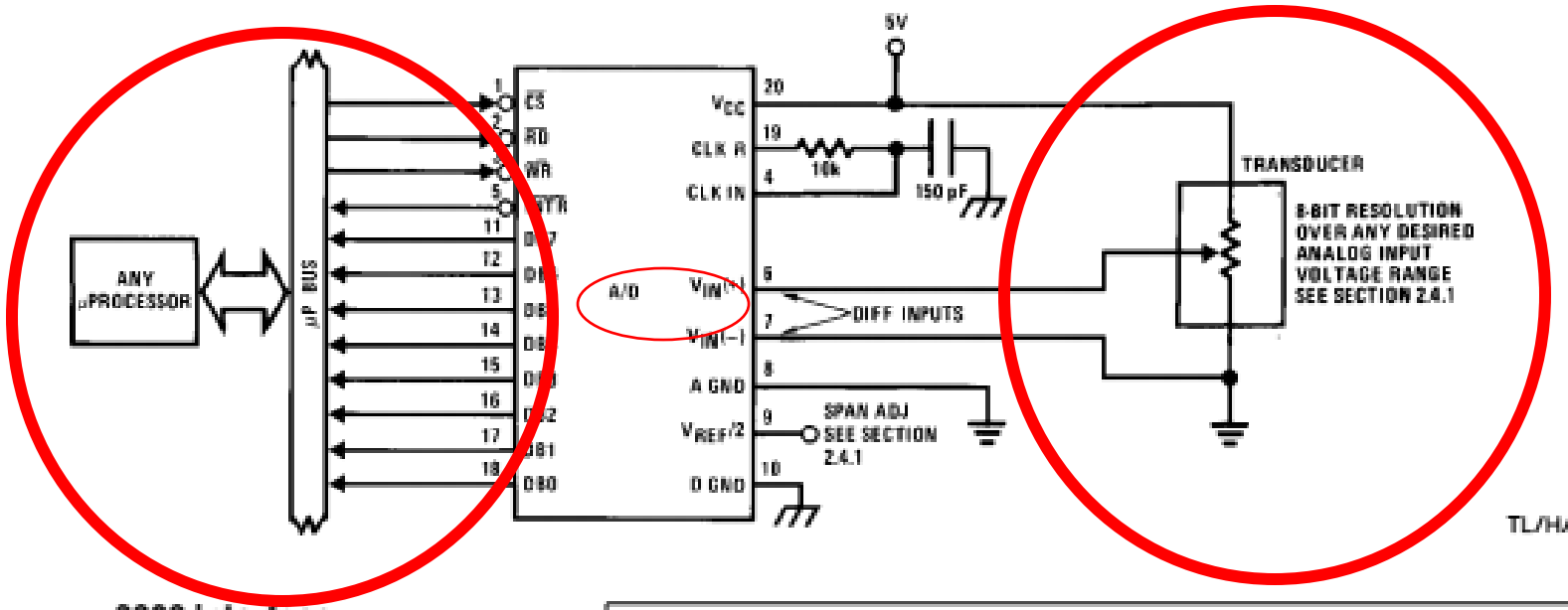
8 bit Binary

Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time . . . . . <100µs
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works with Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- Analog Voltage Input Range (Single + 5V Supply) . . . . . 0V to 5V
- No Zero-Adjust Required
- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required

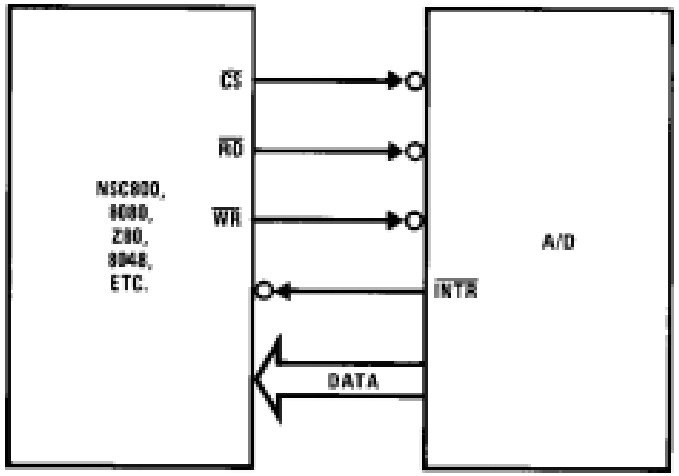
If interrupt==enable ====== WR bar=0 ===== Binary ==== output

Typical Applications



TL/H/5671–1

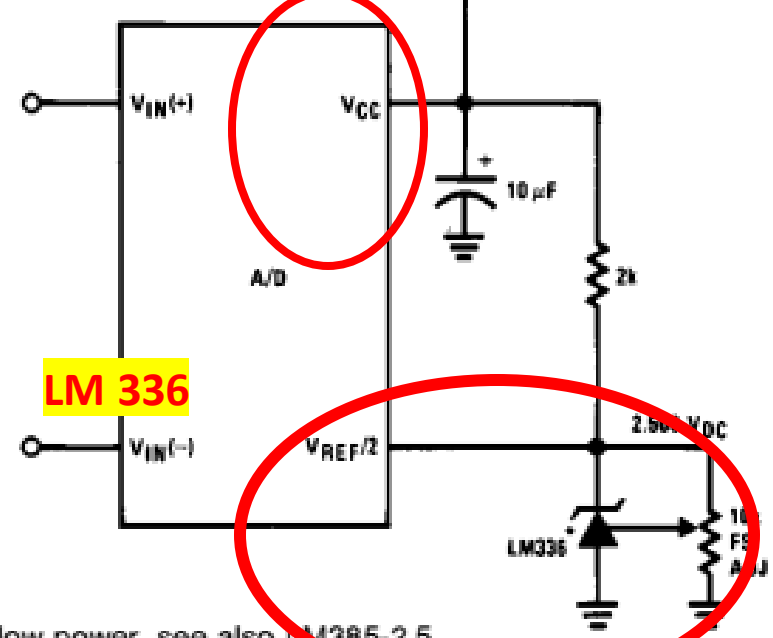
8080 Interface



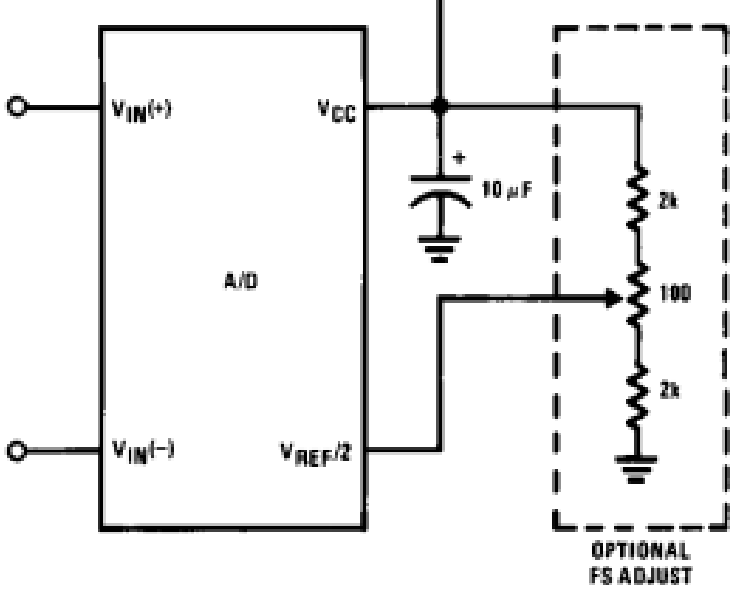
TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	± ¼ LSB		
ADC0802		± ½ LSB	
ADC0803	± ½ LSB		
ADC0804		± 1 LSB	
ADC0805			± 1 LSB

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Z-80® is a registered trademark of Zilog Corp.

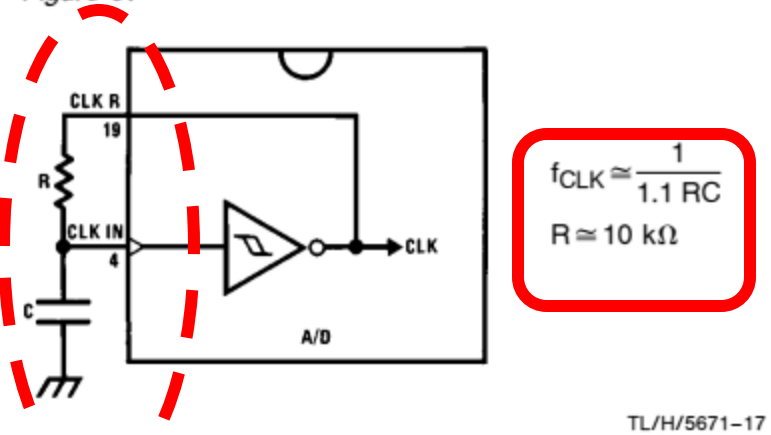


*For low power, see also LM385-2.5



2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \simeq \frac{1}{1.1\ RC}$$

$$R \simeq 10\ k\Omega$$

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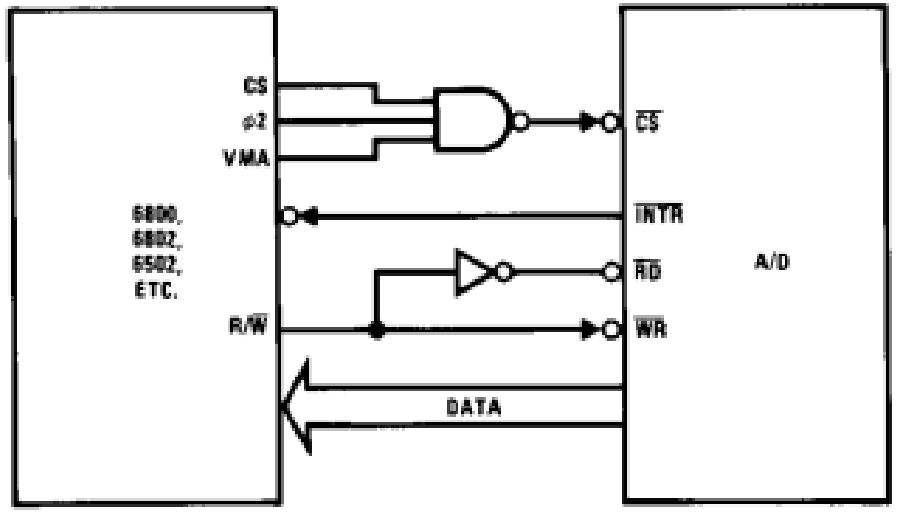
FIGURE 6. Self-Clocking the A/D



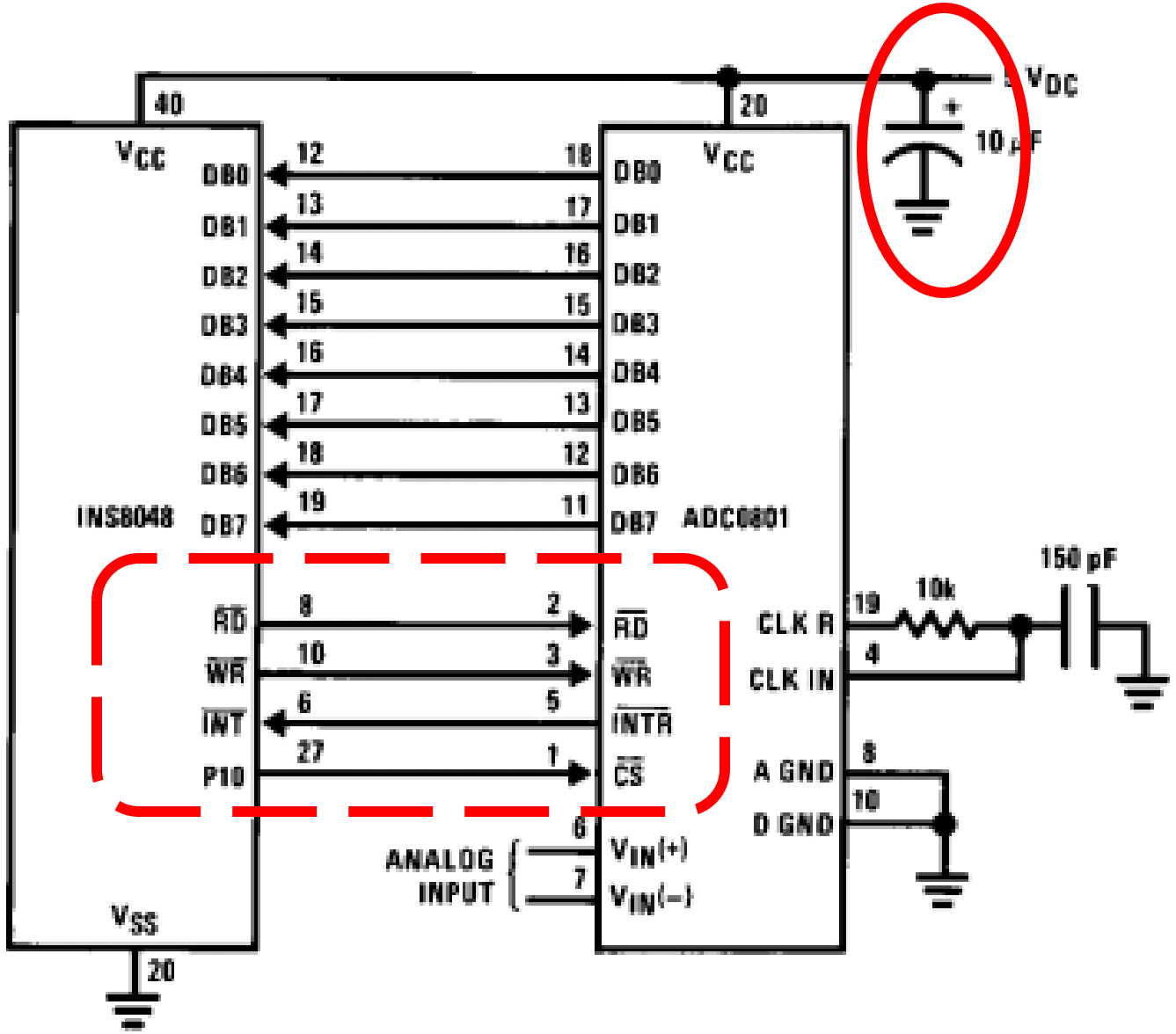


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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

Practice: Proteus implementation

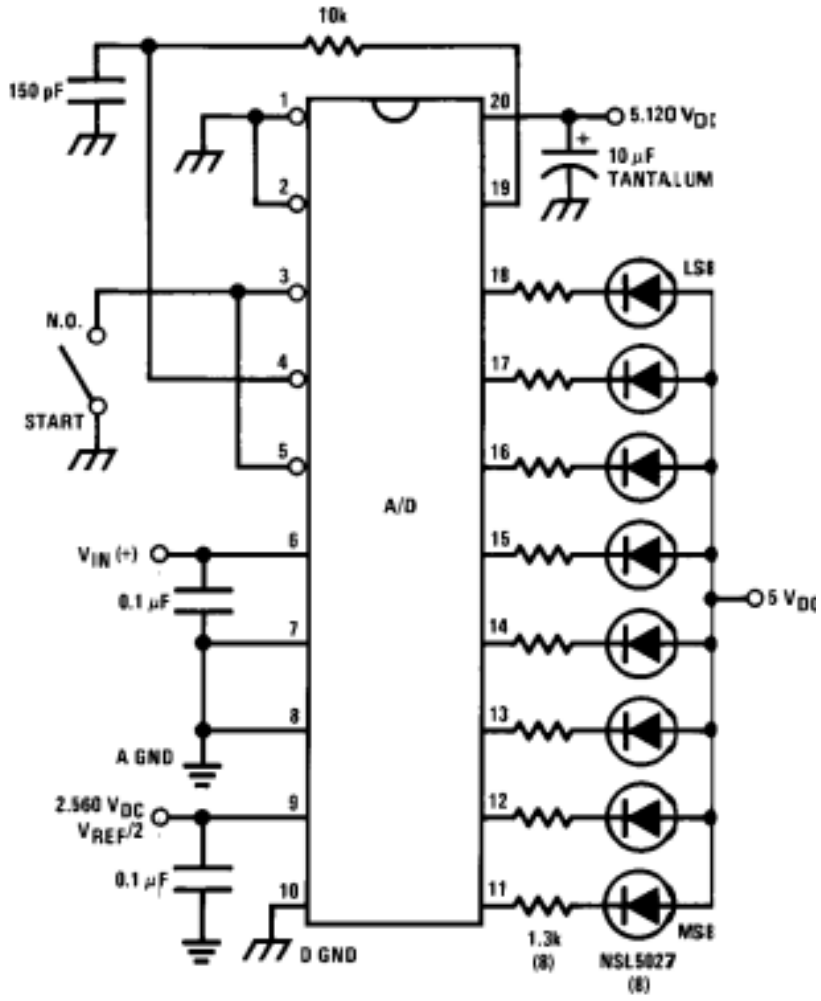

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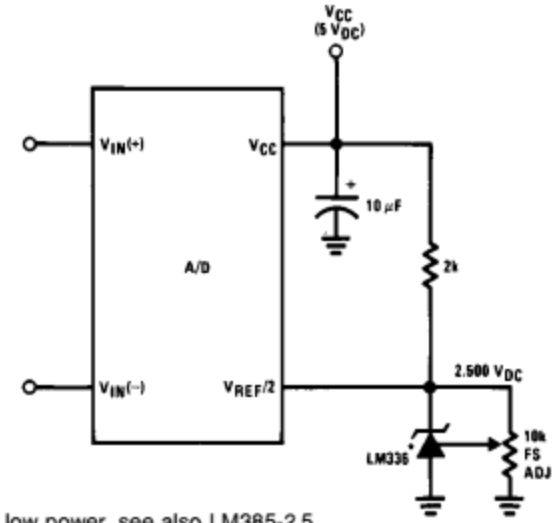
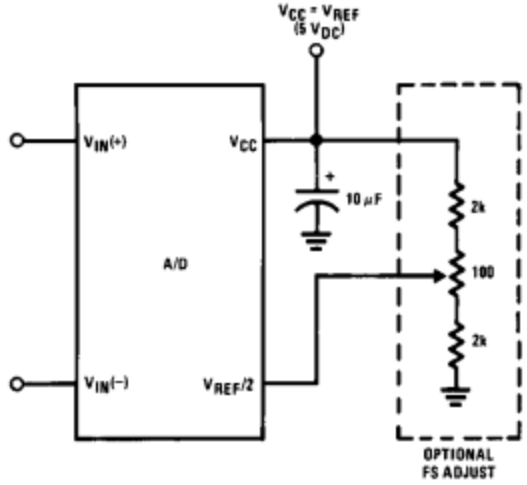
FIGURE 7. Basic A/D Tester

Absolute with a 2.500V Reference

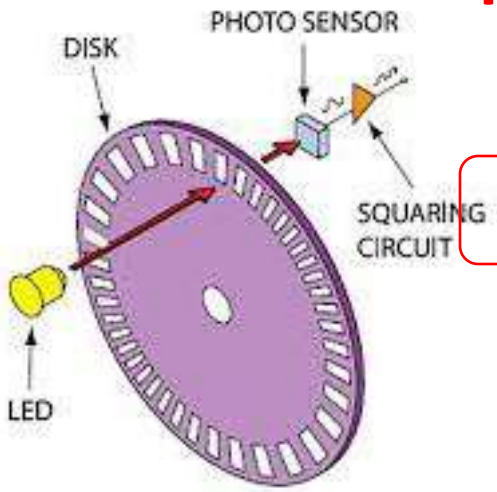


*For low power, see also LM385-2.5

Absolute with a 5V Reference



Incremental encoder



VII. Shaft Encoder

Elctromechanical ADC

- Convert shaft angle to digital output

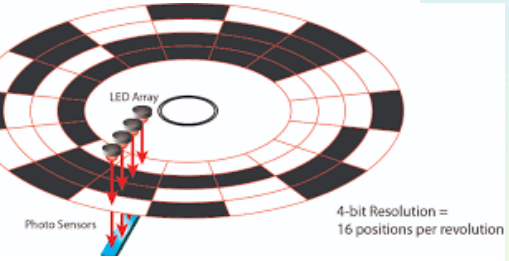
Encoding

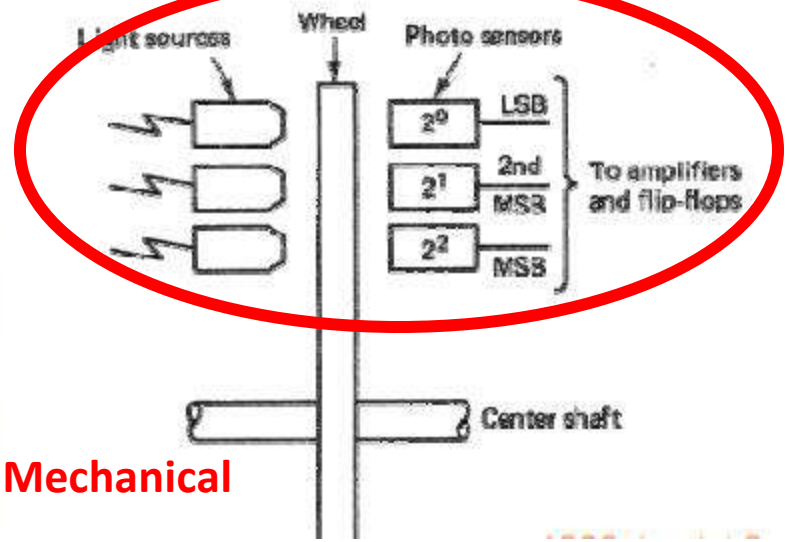
- Optical or Magnetic Sensor

Applications

- Machine tools, Industrial robotics, Numerical control

Absolute encoder

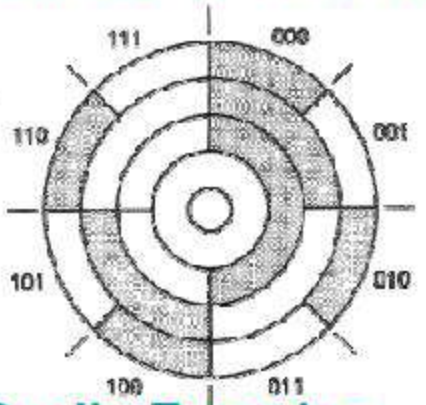




A/D Mechanical

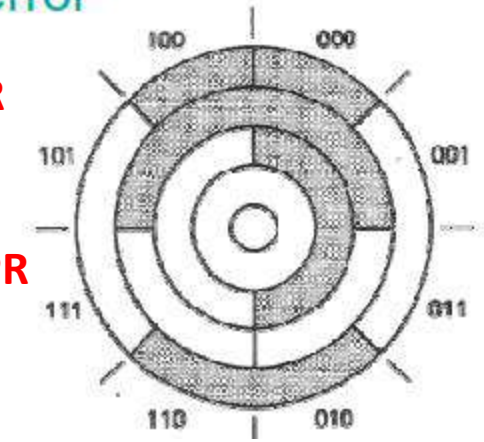
Binary Encoder

- Misalignment of mechanism causes large error
  - Ex: 011 → 111 (180deg)

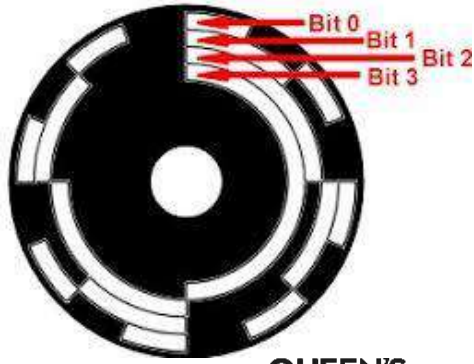


Gray Cyclic Encoder

- Misalignment causes 1 LSB error



1024 PPR
600 PPR
60 PPR
12000 PPR
4 PPR
16 PPR
…



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Thank You For Your Attention!

Any Question?